

WHAT IS CLAIMED IS:

1. A method of generating an ASIC design database, comprising:

5 extracting, when a function design using description data comprising a header portion and an entity portion has been performed, information necessary for reuse design from various execution results of the entity portion;

10 writing the extracted information necessary for reuse design in the header portion of the description data; and

15 storing, as one file at a predetermined location, the description data comprising the header portion in which the information necessary for reuse is written, and the entity portion.

2. A method of generating an ASIC design database, according to claim 1, wherein the information necessary for reuse, which is extracted from the various execution results of the entity portion, is at
20 least a simulation time, layout area, timing, and power consumption.

25 3. A method of generating an ASIC design database, according to claim 1, wherein the entity portion of said description data is described using a hardware description language.

4. A method of generating an ASIC design database, according to claim 1, wherein the entity

portion of said description data is RTL description data described in a register transfer level.

5 5. A method of generating an ASIC design database, according to claim 1, wherein in the file stored at the predetermined location, information written in the header portion and RTL description data in the entity portion are uniformly managed.

6. A method of generating an ASIC design database, comprising:

10 extracting, when a function design using RTL description data comprising a header portion and an entity portion and made in a register transfer level has been performed, information necessary for reuse design from various execution results of the entity
15 portion;

 writing the extracted information necessary for reuse design in the header portion of the RTL description data; and

20 storing, as one file at a predetermined location, the RTL description data comprising the header portion in which the information necessary for reuse is written, and the entity portion.

7. A method of generating an ASIC design database, comprising:

25 performing, when a function design has been carried out by an RTL description composed of a header portion and an entity portion and made in a register

transfer level, a simulation using a simulation tool
with respect to the entity portion of the RTL
description;

5 extracting a simulation time from a simulation
result and writing the simulation time in the header
portion of the RTL description;

10 inputting the entity portion of the RTL
description to a logic synthesis tool and logic-
synthesizing the entity portion, and outputting a gate-
level net list;

 inputting the output gate-level net list to a
timing analysis tool, and outputting a timing analysis
result report;

15 comparing values of the timing analysis result
report with preset conditions;

20 extracting a timing value and a layout area
information, which are the result of the analysis, when
said conditions are met, and writing the extracted
timing value and layout area information in the header
portion of the RTL description;

 performing a logic simulation using a logic
simulation tool with respect to the gate-level net
list;

25 inputting data of the logic simulation to a power
consumption calculation tool, and outputting a power
consumption calculation result;

 extracting a power consumption from the power

